REMARKS

Claims 1-26 are pending in this application. Claim 26 has been newly added.

I. CLAIM REJECTIONS - 35 U.S.C. § 102

No claim is anticipated under 35 U.S.C. §102 (b) unless all of the elements are found in exactly the same situation and united in the same way in a single prior art reference. As mentioned in the **MPEP §2131**, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Every element must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). The identical invention must be shown in as complete detail as is contained in the patent claim. *Id.*, "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970), and MPEP 2143.03.

A. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Kirsten, US 6,011,901. The Applicant respectfully traverses.

1. The Examiner states that concerning claims 1-2, and 8, Kirsten discloses a multi-channel image encoding apparatus and method (figs. 2-5, 8) for selectively receiving image signals

(70) transmitted through a plurality of input channels (cameras 1-8) and encoding (74) the image signals, comprising:

a channel data processor (see col. 9, line 7-40, figs. 4-5, 8: 72, 102 & 104 serve as channel data processor for selectively storing and outputting selected data) comprising a frame buffer group including a plurality of frame buffers for each input channel in order to receive a plurality of frame data through the plurality of input channels and to store the plurality of frame data (i.e. 102, which consists of memory arrays), the channel data processor for selecting data transmitted to the frame buffer group to output the selected data (the selected output data is outputted from 102), the channel data processor storing each unit of the frame data into the frame buffer group corresponding to each channel in accordance with a set-up input channel selection order (col. 9, line 29-35, Note: the field/frame capture consists of memory arrays to store an array of image data in a particular array locations based on an order from selector control 114-see col. 10, line 30-49);

and an encoder for encoding image signals output from the channel data processor with a Moving Picture Experts Group method (74, col. 12, line 52 - col. 13, line 25).

However, Kirsten fails to disclose a frame buffer group including a plurality of frame buffers for each input channel in order to receive a plurality of frame data through the plurality of input channels and to store the plurality of frame data as claimed since reference 102 of Kirsten, which consists of memory arrays fails to disclose such a limitation. In the present invention each one of the input channels includes frame buffers for each input channel, while Kirsten only discloses generally memory arrays. Col. 9, lines 30-32 states "Synchronization data 116 is used to key the

image data into correct array locations." The disclosure is only to key to a correct location, but there is no segregation based on channel on the frame buffers or that the frame buffer group includes a plurality of frame buffers for each input channel as claimed. Respectfully, according to MPEP §2131, the identical invention must be shown in as complete detail as is contained in the patent claim and here such is not disclosed in Kirsten.

2. Concerning claim 1, Kirsten fails to disclose *the channel data processor storing each unit of the frame data into the frame buffer group corresponding to each channel in accordance with a set-up input channel selection order*. Kirsten only discloses "Synchronization data 116 is used to key the image data into correct array locations." Keying image data to correct locations is not identical to storing each of the data into the frame buffer group *corresponding to each channel* in accordance to a setup *input* channel selection order. The relation to channel is not made in the setup and it is not according to input channel selection order. The identical invention is not disclosed as mandated by MPEP §2131.

3. Concerning claim 3, the Examiner states that which further recites "the channel data processor comprising: a first multi-switch unit for selectively contacting each of the input channels with the frame buffer group of corresponding to each of the input channels; and a second multi-switch unit for selectively contacting with the frame buffer group and outputting data output from the frame buffer group to the encoder", Kirsten discloses this aspect (see figs. 4-5 which clearly show

the first and second multi-switch unit as claimed).

The Examiner had stated that 102 and 104 serve as the channel data processor. However, 102 and 104 do not concern selectively contacting each of the input channels. 102 as mentioned in Kirsten, states"A digital field/frame capture 102 receives image data and synchronization data from the video digitizer." Each of the input channels with the frame buffer group is not contacted by 102 or 104.

4. The Examiner states that concerning claim 4, the limitations as claimed have been analyzed and rejected w/r to claims 1 and 3 above.

However, in addition to the comments for claims 1 and 3, additionally, Kirsten fails to disclose the second multiswitch that contacts the frame buffer group according to the setup *channel* contact order. The order in Kirsten is not based on the channel. Rather, as mentioned in Kirsten, "Synchronization data 116 is used to key the image data into correct array locations." Keying to "correct" array locations is not according to the setup channel contact order.

Kirsten mentions the video selector 70 includes "offers an increase in single-field acquisition rates by allowing the invention to control the order of video source selection according to relative phases of the sources." However, the information is not being arranged where there is a plurality of buffers for each input channel. Such connection is not disclosed. Therefore, there not the storing of each unit of frame data into a frame buffer group corresponding to the input channels according to selection order. The corresponding of the buffer to input channel *and* the selection order is not

identically disclosed.

5. Re claim 5, the Examiner states which further recites "the encoder comprising: a discrete cosine transformer for performing a discrete cosine transform with respect to the image signals input from the second multi-switch unit; a quantizer for quantizing signals output from the discrete cosine transformer and outputting the quantized signals; an inverse quantizer for inversely quantizing the quantized signals; an inverse discrete cosine transformer for performing an inverse discrete cosine transform with respect to the inversely quantized signals; a prediction memory; an adder for adding data output from the prediction memory and the inversely discrete cosine transformed data, and outputting the added data to the prediction memory; and a subtracter for subtracting data output from the prediction memory from signals input through the second multi-switch unit, and outputting the subtracted signal to the discrete cosine transformer", Kirsten discloses the above (see figs. 4-5: 74, which also exemplified in details in figs. 11C & 11D, col. 12, line 66 - col. 13, line 25, Note: Kirsten discloses an MPEG encoder which inherently incorporates all of the above limitations of an encoder as claimed).

However, Kirsten does not disclose all of the above limitations, including for example the discrete cosine transformer as arranged in the claim. Kirsten states, "Methods based on transform coding such as DCT (discrete-cosine transform) or wavelet transforms are suitable for compressing surveillance video. JPEG is a DCT-based intraframe technique for still images." However, this is not stating that the DCT performs with respect to the signals input from the *second* multi-switch unit.

A quantizer as arranged in the claims is not disclosed as seen in cols. 11 and 12. General

descriptions are not enough, but the identical invention as arranged in the claim must be disclosed. DCT in general is mentioned, and there is no mention of quantizing the signals from the DCT and then inversely quantized as arranged in the claim.

Further, an inverse DCT is not mentioned specifically as arranged in the claim. There is no mention of such inverse unit. Prediction memory is also not mentioned. The actual structure must be disclosed identically according to MPEP §2131.

6. The Examiner states that regarding claim 6, which further recites "the encoder further comprising: a variable length encoder for performing a variable length encoding with respect to signals output from the quantizer, and outputting the encoded signals; and a parser for loading channel information about each frame to signals output from the variable length encoder, and outputting the signals", again, Kirsten discloses the above (see figs. 4-5: 74, which also exemplified in details in figs. 11C & 11D, col. 12, line 66 - col. 13, line 25, Note: Kirsten discloses an MPEG encoder which inherently incorporates all of the above limitations of an encoder as claimed).

However, a variable length encoder from signals specifically from the quantizer is not disclosed. An encoder is mentioned, but no specific disclosure as to the encoder accommodating variable length and that it encodes the signal from a quantizer.

A parser loading channel information from the variable length encoder is specifically not mentioned in Kirsten as seen in cols 12-13.

7. The Examiner states that regarding claim 9,with respect to the "a prediction memory" as further recited, Kirsten discloses this aspect (see e.g., figs. 11C & 11D, the prediction memory for each respective channel is shown as 208-1 to 208-8).

However, Kirsten states "A 210 selects the previously stored image associated with video stream 1 from image store 1 208-1." This is not disclosing a prediction memory.

8. Concerning claims 15 and 21, the Examiner states that with respect to the "encoder for calculating a similarity by comparing image signals output from the channel data processor and the previous frame data stored in the frame memory provided for corresponding channels, and selecting one mode among a plurality of encoding modes set up differently for each other in regard to the present frame data in accordance with the calculated similarity and encoding according to the selected encoding mode" as claimed, Kirsten also discloses the above (see figs. 11A-11D, col. 12, line 52 - col. 13, line 11. Note: the coding modes are "intraframe" and "interframe" coding modes).

However, as mentioned in Kirsten "Intraframe compression generates a set of data for each original image which, taken alone, sufficiently represents the original image. Intraframe compression is often referred to as still-image compression, as still images are treated independently without relation to other images in the time sequence." In intraframe a comparison is not made and therefore, intraframe cannot be mentioned as the second mode as the claim states that there is a comparison between the images.

As seen in claim 21, the intraframe cannot be used as the similarities have different reference values between the modes.

9. New claim 26 is also not disclosed by Kirsten because Kirsten fails to disclose identically the exclusive allocation of each frame buffer to the channel as relating to the first and second multiswitches. Further, Kirsten fails to disclose the remaining claim as arranged including a first multi-switch unit selectively contacting each one of the input channels with the plurality of frame buffers of the frame buffer group corresponding to each one of the input channels, each one of the input channels corresponding to a specific and exclusive plurality of frame buffers in the frame buffer group; and a second multi-switch unit for selectively contacting with each one of the plurality of frame buffers of the frame buffer group corresponding to each one of the input channels, and outputting data output from the plurality of frame buffers of the frame buffer group corresponding to each one the input channels, to the encoder.

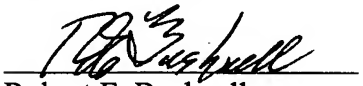
New claim 26 is supported by the drawings in their entirety and the related disclosure, including for example figures 1, 2, 4 and 5.

In view of the foregoing amendments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. If there are any questions, the examiner is asked to contact the applicant's attorney.

A fee of $50 is incurred by this Amendment for the addition of one (1) claim above twenty-five (25). Applicant's check drawn to the order of the Commissioner accompanies this Amendment. Should there be a deficiency in payment, or should other fees be incurred, the Commissioner is

authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



Robert E. Bushnell
Attorney for the Applicant
Registration No.: 27,774

1522 "K" Street N.W., Suite 300
Washington, D.C. 20005
(202) 408-9040

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